FIG. 1

1. MEMORY EMBEDDED SYSTEM LSI

2. INPUT ADDRESS

a. COLUMN

b. ROW

FIG. 2

6. EXTERNAL TEST INPUT ADDRESS

7. LOGIC CIRCUIT

8. NORMAL INPUT ADDRESS

FIG. 3

9. INTERNAL TEST INPUT ADDRESS

10. SIGNAL CONNECTION DIAGRAM

a. TO LOGIC CIRCUIT

FIG. 5

11. ADDRESS SIGNAL CONNECTION CHANGING MEANS

a. INTERNAL COLUMN ADDRESS

b. INTERNAL ROW ADDRESS

FIG. 6

19. SWITCH

20. SWITCH CONTROL SIGNAL

a. TO INTERNAL RAM

b. NOT TO BE USED

FIG. 7

14. FUSE

15. PULL-DOWN RESISTOR

FIG. 8

(a1) WRITE "0" TO CELLS TO 1.0 - 1 Mb AREA

(a3) READ "0" AND WRITE "1" ON EACH CELL IN 3.0 Mb - 1 Mb AREA

(A4) FULL CAPACITY MACRO FAILS HERE

FIG. 9

a. MEMORY BLOCK

18. INTERNAL TEST INPUT ADDRESS (FOR ACCESSING VIRTUAL MEMORY SPACE)

20. COLUMN DECODE SIGNAL

23. ROW DECODE CIRCUIT

24. COLUMN DECODE CIRCUIT

25. ROW DECODE SIGNAL

27. VIRTUAL MEMORY SPACE DECODE